What is claimed is:

1. A D/A conversion circuit for supplying to an output line a gradation voltage corresponding to n-bit digital signal (n is a natural number that is equal to or larger than 2) to be input,

wherein the n-bit digital signal is divided into upper x bit(s) and lower y bit(s) (where $x + y = n$; both x and y are natural numbers),

wherein adjacent two gradation voltage lines among (2^x+1) gradation voltage lines are selected in accordance with the upper x bit(s) of the n-bit digital signal,

wherein after a first gradation voltage applied to either one of the selected adjacent two gradation voltage lines is supplied to the output line, 2^y second gradation voltages are generated from a potential difference between the selected adjacent two gradation voltage lines by the lower y bit(s) of the n-bit digital signal, and

wherein one of the 2^y second gradation voltages is supplied to the output line.

2. A circuit according to claim 1, wherein the D/A conversion circuit is manufactured on an insulating substrate by using a thin film transistor.

3. A circuit according to claim 1, wherein the first gradation voltage is lower than a voltage value applied to the other one of the selected adjacent two gradation voltage lines.

4. A D/A conversion circuit for supplying to an output line a gradation voltage

corresponding to n-bit digital signal (n is a natural number that is equal to or larger than 2) to be input,

wherein the n-bit digital signal is divided into upper x bit(s) and lower y bit(s) (where $x + y = n$; both x and y are natural numbers),

wherein the z-th and (z+1)-th gradation voltage lines among (2^x+1) gradation voltage lines are selected in accordance with the upper x bit(s) of the n-bit digital signal (where z is a natural number in the range from 1 to 2^x),

wherein after a first gradation voltage applied to either one of the selected z-th and (z+1)-th gradation voltage lines is supplied to the output line, 2^y second gradation voltages are generated from a potential difference between the selected z-th and (z+1)-th gradation voltage lines by the lower y bit(s) of the n-bit digital signal, and

wherein one of the 2^y second gradation voltages is supplied to the output line.

5. A circuit according to claim 4, wherein the D/A conversion circuit is manufactured on an insulating substrate by using a thin film transistor.

6. A circuit according to claim 4, wherein the first gradation voltage is lower than a voltage value applied to the other one of the selected adjacent two gradation voltage lines.

7. A semiconductor device, comprising:

a plurality of TFTs arranged in matrix; and

a source signal line driver circuit and a gate signal line driver circuit both

for driving the plurality of TFTs,

wherein the source signal line driver circuit comprises a D/A conversion circuit for supplying to an output line a gradation voltage corresponding to n-bit digital signal (n is a natural number that is equal to or larger than 2) to be input,

wherein the n-bit digital signal is divided into upper x bit(s) and lower y bit(s) (where $x + y = n$; both x and y are natural numbers),

wherein adjacent two gradation voltage lines among (2^x+1) gradation voltage lines are selected in accordance with the upper x bit(s) of the n-bit digital signal.

wherein after a first gradation voltage applied to either one of the selected adjacent two gradation voltage lines is supplied to the output line, 2^y second gradation voltages are generated from a potential difference between the selected adjacent two gradation voltage lines by the lower y bit(s) of the n-bit digital signal, and

wherein one of the 2^y second gradation voltages is supplied to the output line.

8. A device according to claim 7, wherein the plurality of TFTs, the source signal line driver circuit, and the gate signal line driver circuit are integrally manufactured on an insulating substrate by using a thin film transistor.

9. A device according to claim 7, wherein the first gradation voltage is lower than a voltage value applied to the other one of the selected adjacent two gradation voltage lines.

10. A semiconductor device, comprising:

a plurality of TFTs arranged in matrix; and

a source signal line driver circuit and a gate signal line driver circuit both for driving the plurality of TFTs,

wherein the source signal line driver circuit comprises a D/A conversion circuit for supplying to an output line a gradation voltage corresponding to n-bit digital signal (n is a natural number that is equal to or larger than 2) to be input,

wherein the n-bit digital signal is divided into upper x bit(s) and lower y bit(s) (where $x + y = n$; both x and y are natural numbers),

wherein the z-th and (z+1)-th gradation voltage lines among (2^x+1) gradation voltage lines are selected in accordance with the upper x bit(s) of the n-bit digital signal (where z is a natural number in the range from 1 to 2^x),

wherein after a first gradation voltage applied to either one of the selected z-th and (z+1)-th gradation voltage lines is supplied to the output line, 2^y second gradation voltages are generated from a potential difference between the selected z-th and (z+1)-th gradation voltage lines by the lower y bit(s) of the n-bit digital signal, and

wherein one of the 2^y second gradation voltages is supplied to the output line.

11. A device according to claim 10, wherein the plurality of TFTs, the source signal line driver circuit, and the gate signal line driver circuit are integrally manufactured on an insulating substrate by using a thin film transistor.

12. A device according to claim 10, wherein the first gradation voltage is lower than a voltage value applied to the other one of the selected adjacent two gradation voltage lines.

13. A semiconductor device, comprising:

a plurality of TFTs; and

a source signal line driver circuit and a gate signal line driver circuit both for driving the plurality of TFTs,

wherein the source signal line driver circuit comprises a D/A conversion circuit for supplying to an output line a gradation voltage corresponding to n-bit digital signal (n is a natural number that is equal to or larger than 2) to be input,

wherein the n-bit digital signal is divided into upper x bit(s) and lower y bit(s) (where $x + y = n$; both x and y are natural numbers),

wherein the z-th and (z+1)-th gradation voltage lines among (2^x+1) gradation voltage lines are selected in accordance with the upper x bit(s) of the n-bit digital signal (where z is a natural number in the range from 1 to 2^x),

wherein after a first gradation voltage applied to either one of the selected z-th and (z+1)-th gradation voltage lines is supplied to the output line, 2^y second gradation voltages are generated from a potential difference between the selected z-th and (z+1)-th gradation voltage lines by the lower y bit(s) of the n-bit digital signal, and

wherein one of the 2^y second gradation voltages is supplied to the output line.

14. A device according to claim 13, wherein the plurality of TFTs, the source signal line driver circuit, and the gate signal line driver circuit are integrally manufactured on an insulating substrate by using a thin film transistor.

15. A device according to claim 13, wherein the first gradation voltage is lower

than a voltage value applied to the other one of the selected adjacent two gradation voltage lines.

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